REMARKS

Claims 1-3, 5-7, 9, 10 and 12-14 are pending in the present application. Claims 5, 9, 12 and 14 have been amended. Claims 8, 11 and 15 have been canceled.

Drawings

Applicant notes the Examiner's acceptance of the corrected formal drawings as filed along with the Amendment dated October 9, 2003.

Claim Rejections-35 U.S.C. 103

Claims 5-7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishimoto reference (U.S. Patent No. 5,289,036) in view of the Takao et al. reference (Japanese Patent Publication No. 2000-183214) and the Yamaji et al. reference (U.S. Patent No. 6,198,165). Also, claim 8 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art as relied upon with respect to claims 5-7, and in further view of the Ogawa et al. reference (U.S. Patent No. 6,237,218). These rejections, insofar as they may pertain to the presently pending claims, are traversed for the following reasons.

The chip-size semiconductor package of claim 5 includes in combination a connecting portion "directly between the conductive wiring pattern and the conductive post, the connecting portion having a width that gradually decreases from a first boundary at the conductive post to a second boundary at the conductive wiring pattern",

and a dummy pattern "arranged adjacent the first and second boundaries and along sides of the connecting portion". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

The connecting portion of claim 5 is featured as being located directly between a first boundary at the conductive post and a second boundary at the conductive wiring pattern, wherein a width of the connecting portion gradually decreases from the first boundary at the conductive post to the second boundary at the conductive wiring pattern. The dummy portion is thus featured as adjacent the first boundary at the conductive post and the second boundary at the conductive wiring pattern, and along sides of the connecting portion. Also, the connecting portion of gradually decreasing width is directly connected to the conductive post at the first boundary. Although not necessarily limited thereto, these features can be appreciated in consideration of area 340, conductive post 320 and dummy patterns 350 in Fig. 6 of the present application.

In Figs. 2A and 2B of the Ogawa et al. reference as relied upon by the Examiner, the connecting portion of gradually decreasing width is connected directly to via land 21, not conductive pillar 23. The Ogawa et al. reference thus fails to disclose the connecting portion of claim 5 which is directly connected between a first boundary at a conductive post and a second boundary at a conductive wiring pattern, and wherein a width of the connecting portion gradually decreases from the first boundary (conductive post) to the second boundary (conductive wiring pattern). The prior art as relied upon by the Examiner thus fails to disclose or make obvious all the features of claim 5.

Applicant therefore respectfully submits that the chip-size semiconductor package of claim 5 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these rejections, insofar as they may pertain to claims 5-7, are improper for at least these reasons.

With further regard to this rejection, the Yamaji et al. reference as illustrated in Figs. 1 and 2 includes external connection terminals 5 which are solder bumps and which are connected to external connection region 10 of wiring pattern 8, as described in column 5, lines 66-67 and column 6, lines 20-23. The Yamaji et al. reference as relied upon by the Examiner does not include a conductive post in addition to a terminal, as would be necessary to meet the features of claim 5. Since the Yamaji et al. reference does not include a conductive post, dummy wiring patterns 14 as illustrated in Fig. 2 in particular are not featured as adjacent a first boundary of a connecting portion at a conductive post, as featured in claim 5. Thus, the Yamaji et al. reference does not disperse thermal expansion stress of a connecting portion at a conductive post as in the present application. Applicant therefore respectfully submits that the chip-size semiconductor package of claim 5 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these rejections, insofar as they may pertain to claims 5-7, are improper for at least these additional reasons.

Claims 9 and 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishimoto reference in view of the Takao et al. reference, in

further view of the Bertolet et al. reference (U.S. Patent No. 5,844,317). Claim 11 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art as relied upon with respect to claims 9 and 10, and in further view of the Ogawa et al. reference. Applicant respectfully submits that these rejections, insofar as they may pertain to the presently pending claims, are improper for at least the following reasons.

As emphasized previously, the Ogawa et al. reference does not disclose or make obvious a connecting portion as featured in claim 9, that is located directly between a first boundary at a conductive post and a second boundary at a conductive wiring pattern, wherein a width of the connecting portion gradually decreases from the first boundary (conductive post) to the second boundary (conductive wiring pattern). That is, the wiring pattern in Figs. 2A and 2B of the Ogawa et al. reference are directly connected to via land 21, not conductive pillar 23.

Moreover, the dent of claim 9 is featured in combination as "formed at and around the connecting portion". That is, the dent is formed at the connecting portion that has gradually decreasing width. However, conductive strap 16 as illustrated in Figs. 1 and 2 of the Bertolet et al. reference is described in column 8, lines 19-22 as having a tapered width from a middle section 30 to end 22 beneath test protrusion 20. Although this section of conductive strap 16 is described as having a tapered width, a decreasing width is not illustrated in Fig. 1. Regardless, aperture 13 (interpreted as the dent by the Examiner) is not located at the so-called "tapered" width section of conductive strap 16, as would be necessary to meet the features of claim 9. The prior

art as relied upon by the Examiner thus does not disclose or make obvious all the features of claim 9. Applicant therefore respectfully submits that the chip-size semiconductor package of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these rejections, insofar as they may pertain to claims 9 and 10, are improper for at least these reasons.

Claims 12-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishimoto reference in view of the Takao et al. reference, in further view of the Galloway reference (U.S. Patent No. 5,886,414). Also, claim 15 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art as relied upon with respect to claims 12-14, and in further view of the Ogawa et al. reference. These rejections, insofar as they may pertain to the presently pending claims, are traversed for the following reasons.

As noted above, the Ogawa et al. reference as relied upon by the Examiner does not disclose or make obvious the connecting portion as featured in claim 12.

Moreover, the connecting portion of claim 12 is featured in combination as "having a first region extending outwardly from the conductive post and a second region extending in a perpendicular direction from the first region, the second region extending from the connecting portion". In other words, the second region extends from the connecting portion that is located between the first boundary at the conductive post and the second boundary at the conductive wiring pattern, whereby a width of the connecting portion gradually decreases from the first boundary (conductive post) to the

second boundary (conductive wiring pattern).

The Examiner has apparently interpreted the horizontally extending portions of extension areas 60 in Figs. 6B and 7 as the second region of claim 12. However, these portions of extension areas 60 in Figs. 6B and 7 of the Galloway reference do not extend from a connecting portion that is located between a first boundary at a conductive post and a second boundary at a conductive wiring pattern, and which has a width that gradually decreases. That is, narrow region 62 of the Galloway reference has apparently been interpreted by the Examiner as the connecting portion of claim 12. Narrow region 62 however does not have gradually decreasing width, and extension areas 60 do not extend therefrom. The prior art as relied upon by the Examiner therefore fails to meet all the features of claim 12. Applicant therefore respectfully submits that the chip-size semiconductor package of claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these rejections, insofar as they may pertain to claims 12-14, are improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 1-3 are allowed.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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